**In the Specification:**

Please replace paragraph [0016] with the following amended paragraph:

[0016] At this point, the via 102 will be mostly filled with the heavily doped metal alloy 120 as shown in FIG. 1d. As EM problems are frequently localized at the via 102 locations, so the high dopant content of this intermediate metal layer [[110]] 120 is perfectly suited to minimize those EM problems. It is understood that the chip design rules for maximum electrical current density and maximum sheet resistance for this current level may make either the EM of the vias or the resistance (per unit length) of these minimum-width lines to be the tighter constraint. In case that the EM of the vias is the tighter restraint, it would be advantageous for these minimum vias and/or lines to be on the order of twice the thickness of the intermediate layer [[110]] 120 as shown in FIG. 1d.

Please replace paragraph [0018] with the following amended paragraph.

[0018] It is also understood that although the main layer of Cu is deposited without interrupting the standard deposition process, alternatively, this main layer 130 could be formed by using a separate deposition/plating step (probably using a separate ECP apparatus). In essence, this main layer of Cu 130 should have a desired minimum thickness to provide a conductive layer of a low enough electrical resistance plus a safe margin to allow for the future

CMP step. And for that reason, the main layer 130 is generally thicker than the intermediate layer 120, as shown in FIGs. 1e, 1f, and 1g.